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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,548	12/17/2001	Arvind Halliyal	AF01120	5462

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Thomas W. Adams  
Renner, Otto, Boisselle, & Sklar, L.L.P.  
19th Floor  
1621 Euclid Avenue  
Cleveland, OH 44115

EXAMINER

KIELIN, ERIK J

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 09/17/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicant(s)

10/023,548

Applicant(s)

HALLIYAL ET AL.

Examiner

Erik Kielin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 July 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 2-4, 14-16 and 18-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 5-13 and 17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election of the species of group I, claims 1, 5-13, and 17, in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 2-4 and 14-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.
3. Examiner acknowledges Applicant's comments regarding claim 22. As will be noted below the claims appear to have been incorrectly numbered. Specifically, number "19" was skipped in the claim numbering. Accordingly, there exist only 21 claims in the instant application. There is no claim 22 of record.

### ***Claim Objections***

4. The numbering of claims is improper for not being consecutive. Specifically, the claims were numbered 18, 20, 21, and 22 instead of 18, 19, 20, and 21. Mis-numbered claims 20, 21, and 22 have been renumbered 19, 20, and 21, respectively. Claims 5 and 6 are objected to because of the following informalities:

in the first line of each claim, replace "an oxide" with --a first oxide-- for consistency with the antecedent. Appropriate correction is required.

***Specification***

6. The disclosure is objected to because of the following informalities:
- on p. 6, line 18, after “also” insert --to-- for clarity;
- on p. 7, lines 4 and 6, replace “34” with --34a and 34b-- for consistency with the Fig. 1.
- Appropriate correction is required.

***Drawings***

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 10, 36, and 40.
8. Fig. 1 is objected to because the drawings are not consistent with the specification. The specification, in the paragraph bridging pages 6 and 7 indicates that the charges 34a and 34b are stored in the nitride layer 30, but the charges are shown in the oxide layer 28.
9. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:
- The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
11. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 requires that the formation of the dielectric stack be "carried out in an RTP and RTCVD chamber." The claim is considered indefinite because, as presently written, it is unclear whether these are the same or separate chambers, or whether the chambers are alternatives. For the purposes of patentability, the chambers will be considered as alternatives, the broadest interpretation.

*Claim Rejections - 35 USC § 103*

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 1, 5-9, 12, 13, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,953,254 (**Pourkeramati**) in view of **Van Zant**, Microchip Fabrication, 4th ed. McGraw-Hill: New York, 2000, pp. 172-173, 179-182, 480-487.

Regarding claim 1, **Pourkeramati** discloses a process for fabrication of a semiconductor device including an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate **214** having a silicon surface **202** (Figs. 3);  
forming a first oxide layer **203** on the silicon surface;  
depositing a silicon nitride layer **204** about 75-90 Å thick on the first oxide layer; and  
forming a top oxide layer **205** of 30-50 Å thick on the silicon nitride layer, wherein the top oxide layer **205** is formed by a wet oxidation of a surface of the silicon nitride layer **204** (col. 5, lines 15-23).

**Pourkeramati** does not indicate the method by which the wet oxidation is performed.

**Van Zant** teaches that the preferred method of performing wet oxidation for cleanliness and control of the process is by providing a mixture of hydrogen (H<sub>2</sub>) and oxygen (O<sub>2</sub>) which react in the chamber (i.e. *in situ*) to form water as steam. (See pp. 172-173.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the ISSG method of forming steam for the wet oxidation of **Pourkeramati** for the beneficial reasons just indicated in **Van Zant**.

Regarding claims 5, 6, and 8, the claims state that the dielectric stack is "carried out in an RTP and RTCVD chamber" (claims 5 and 8) or is "carried out in a single-wafer cluster tool" (claims 6 and 8). These limitations are not considered to have patentable weight because it has been held that to be entitled to weight in method claims, the recited structure limitations therein must affect the method in a manipulative sense, and not amount to the mere claiming of a use of a particular structure. See Ex parte Pfeiffer, 1962, C.D. 408 (1961). In the instant case, the apparatus in which the oxide/nitride/oxide stack is formed is not manipulative of the method.

If it is thought somehow that the structure limitations are manipulative of the invention, then this may be a difference. **Van Zant** teaches the benefits of using RTP, RTP-CVD (pp. 179-181), and cluster tools (pp. 480-481).

Further in regard to claim 5, **Van Zant** teaches that RTP, in general, is beneficial for reducing the thermal budget in the formation of semiconductor devices (p. 180, first sentence). On p. 181, **Van Zant** particularly states that rapid thermal wet (steam) oxidation is known and also states that RTP-LPCVD of silicon nitride is known. It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the dielectric stack

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(oxide/nitride/oxide) of **Pourkeramati** in an RTP and RTCVD chamber to take advantage of the beneficial reduction in thermal budget, as taught by **Van Zant**.

Further in regard to claim 6, **Van Zant** teaches that clustering tools for automation of process steps reduces time and improves cleanliness and makes better products (i.e. semiconductor devices). (See p. 481.) **Van Zant** also teaches the benefits of using a single wafer cluster tool on p. 486, indicating that single wafer apparatus provides better uniformity and easier process control for larger wafers than does batch wafer processing. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the semiconductor device of **Pourkeramati** in a single-wafer cluster tool to take advantage of easier processing, better uniformity, improved cleanliness, and better products, each as taught by **Van Vant**.

Further in regard claim 8, it would be obvious to one of ordinary skill to provide hydrogen and oxygen to the RTP or single-wafer cluster tool to perform the wet oxidation of **Pourkeramati** because **Van Zant** teaches that *in-situ* generation of steam is cleaner and better controlled and because cluster tools and/or RTP tools provide better control of processes with reduced thermal budget, as just noted above.

Regarding claim 7, although **Pourkeramati** does not teach the method by which the nitride layer is deposited, **Van Zant** teaches the RTP-LPCVD of nitride is beneficial for, at least, reducing the thermal budget over non-RTP methods. It would have been obvious for one of ordinary skill in the art, at the time of the invention to deposit the nitride layer of **Pourkeramati** by RTCVD, as taught by **Van Zant**, to reduce the thermal budget in the fabrication of the semiconductor device.

Regarding claim 9, as noted above, **Pourkeramati** uses the claimed temperature for the wet oxidation, 1000 °C.

Regarding claims 12 and 13, the thicknesses in **Pourkeramati** fall within or touch the claimed thicknesses for the silicon nitride and top oxide layers, as noted above.

Regarding claim 17, it would be obvious to one of ordinary skill to provide hydrogen and oxygen to the RTP or single-wafer cluster tool to perform the wet oxidation of **Pourkeramati** which is performed at 1000 °C, as noted above, because **Van Zant** teaches that *in-situ* generation of steam is cleaner and better controlled and because RTP tools beneficially provide reduced thermal budget, as noted above in regard to claims 5, 6, and 8.

14. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable **Pourkeramati** in view of **Van Zant** as applied to claim 1 above, and further in view of US 6,271,054 B1 (**Ballantine et al.**).

Regarding claim 10, the prior art of **Pourkeramati** in view of **Van Zant**, as explained above, discloses each of the claimed features except for indicating the RTCVD conditions of 0.5 to 2 slm ammonia and 20 to 50 sccm silane or dichlorosilane.

**Ballantine** teaches a method of forming a silicon nitride layer using, inter alia, silane or dichlorosilane and ammonia (col. 3, lines 45-48). **Ballantine** teaches that the ratio of flow rates of the silicon-containing compound to ammonia varies from 1:25 to 1:400 (col. 3, lines 50-54) and teaches flow rates of ammonia of about 1 to 10 slm (called "l/min"; col. 3, lines 65-67) which overlaps the instant flow rates and ratios. In other words, if 2 slm of ammonia is used then 5 to 80 sccm of silane or dichlorosilane would be used.



It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the RTCVD deposition conditions of **Ballantine** in the method of **Pourkeramati** in view of **Van Zant**, because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. See In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). One of ordinary skill would be motivated to optimize standard RTCVD silicon nitride conditions to form the best nitride layer for a given application.

Regarding claim 11, note that **Van Zant** teaches on page 180, Fig. 7-27 shows that a typical RTP cycle includes at least a temperature ramp up step to the desired RTP temperature, a dwell period at the given temperature, and a cool down period. It would have been obvious for one of ordinary skill in the art, at the time of the invention to use ramp up, dwell, and cool down periods as **Van Zant** teaches that these are notoriously well known steps, required in any RTP process.

Further regarding claim 11, although the exact time of 2 minutes is not taught, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to select the appropriate time to deposit the silicon layer to the desired thickness depending upon the RTCVD conditions used. See In re Jones and In re Boesch, *supra*. Because **Pourkeramati** teaches the desired thickness of the silicon nitride layer, which reads-on the instantly claimed thicknesses, one of ordinary skill would know to optimize the conditions of flow rate and time to form the silicon layer to the indicated thickness.

*Conclusion*

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

JP 4-42568 (**Honda**) teaches and ONO stack, wherein the top oxide is formed by wet oxidation of the nitride layer. (See Abstract.)

US 6,058,045 (**Pourkeramati**) is a patent issuing from a divisional application of that application issued to **Pourkeramati** cited above.

US Patent Application 2001/0012667 A1 (**Ma et al.**) teaches a cluster tool for forming gate oxides wherein RTP and RTCVD chambers are included in the cluster tool. (See at least paragraph [0019].)

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached at 703-306-2417. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

  
Erik Kielin

September 13, 2002